SAULT COLLEGE OF APPLIED ARTS AND TECHNOLOGY

SAULT STE. MARIE, ONTARIO

Sault College

COURSE OUTLINE

COURSE TITLE: **Microprocessor Circuits and Systems**

CODE NO. : **CST200** SEMESTER: **4**

PROGRAM: **Computer Engineering Technology**

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DATE: **Jan, 2002** PREVIOUS OUTLINE DATED: **Jan, 2001**

APPROVED:

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DEAN DATE

TOTAL CREDITS: **4**

PREREQUISITE(S): **CST100, CST202**

HOURS/WEEK: **4**

Microprocessor Circuits and Systems **CST200**
Course Name Code No.

I. COURSE DESCRIPTION:

This course will introduce the student to microprocessor circuits and systems and the peripheral devices used to support them, as well as strengthen his/her knowledge of digital devices in general. Microcomputer system hardware components will be studied and practical lab exercises, based on the Intel processor and the ISA bus, will reinforce the theory. The essential principles of operation of microprocessor-based systems are approached from the point of view of modifying and designing interfaces for them, and writing software routines to test and control them.

II. A LEARNING OUTCOMES:

Upon successful completion of this course, the student will demonstrate the ability to:

1. Describe the organisation of typical microprocessor systems as implemented with address, data and control busses.

2. Describe the operation of the 8088 microprocessor in detail, including the various support chips required in typical microprocessor-based systems.

3. Describe the different types of memory devices found in computer systems, their advantages and disadvantages, principles of operation.

4. Describe and build memory and I/O address decoders.

5. Utilise an Analogue-to-Digital and Digital-to-Analogue converter to digitise and reconstruct an analogue signal.

6. Implement techniques of I/O interfacing including handshaking, polling, interrupts, DMA and describe the operation of the devices used to support these methods.

7. Utilise a Logic Analyser to analyse bus traffic within a Microprocessor based system.

II. B LEARNING OUTCOMES AND ELEMENTS OF THE PERFORMANCE:

Upon successful completion of this course, the student will demonstrate the ability to:

1. Describe the organisation of typical microprocessor systems as implemented with address, data and control busses.

Potential Elements of the Performance:

- Describe the general nature and detailed operation of address, data and control busses in microcomputer systems.
- Describe and construct circuits that utilise flip-flops, buffers and transceivers in computer systems.
- Discuss the need for 3-state logic and the use of 3-state devices in computer systems in general.

This learning outcome will constitute approximately 10% of the course.
Reference: Text Chap. 7

2. Describe the operation of the 8088 microprocessor in detail, including the various support chips required in typical microprocessor-based systems.

Potential Elements of the Performance:

- Describe the 8088 CPU, internal organisation, pin functions and operating modes.
- Describe how bus multiplexing is accomplished.
- Describe the 8088 timing diagram and be able to use a logic analyser to demonstrate this understanding.
- Describe the role of the 8284 Clock Generator and the 8288 Bus Controller

This learning outcome will constitute approximately 10% of the course.
Reference: Text Chap. 9

3. Describe the different types of memory devices found in computer systems, their advantages and disadvantages, principles of operation.

Potential Elements of the Performance:

- Identify the principal types of static (SRAM) and dynamic (DRAM) Read/Write Memory (RWM or RAM) and describe their features, operation, advantages and disadvantages and their implementation in memory systems.
- examine the characteristics of state-of-the-art memory devices used in personal computers today and describe their advantages over older devices
- Describe the characteristics of various ROM,(Read-Only Memory devices), PROMs,EPROMs, and EEPROMs and understand the process of EPROM

programming.
- Describe the characteristics of various Programmable Logic Devices (PLD's), PLAs, PAL's and ASICs.

This learning outcome will constitute approximately 10% of the course.
Reference: Text Chap. 11

4. Describe and build memory and I/O address decoders.

Potential Elements of the Performance:
- analyse and/or design an address decoder utilising the 74138 to selectively enable memory or I/O devices.
- Describe the use of memory maps, memory mapped I/O and dedicated I/O

This learning outcome will constitute approximately 20% of the course.
Reference: Text Chap. 12.

5. Utilise an Analogue-to-Digital and Digital-to-Analogue converter to digitise and reconstruct an analogue signal.

Potential Elements of the Performance:
- Describe the nature of an A/D and D/A converter
- Draw the block diagram of a system utilising an A/D and D/A
- Write a program to utilise an A/D and D/A converter.

This learning outcome will constitute approximately 15% of the course.
Reference: ch12, Handouts.

6. Implement I/O interfacing techniques including handshaking, polling, interrupts, DMA and describe the devices used to support these methods.

Potential Elements of the Performance:
- Implement hardware handshaking in order to perform a parallel data transfer between two computers
- Describe the difference in nature between polled I/O, interrupt I/O and DMA
- Describe the role of the 8259 Programmable Interrupt Controller (PIC) and the sequence of events that occur during an Interrupt event
- Develop an interrupt based software interface (driver) for the a/d converter
- Describe the role of the 8237 DMA controller and the sequence of events in a DMA transfer
- Describe the 8253 Programmable Interval Timer (PIT), its operation and function.

This learning outcome will constitute approximately 20% of the course.
Reference: Text Chap.13,14,15

7. Utilise a Logic Analyser to analyse bus traffic within a Microprocessor based system.

Potential Elements of the Performance:

- capture and display the signal traffic as it travels along the address, data and control bus during an I/O or Memory data transfer cycle

This learning outcome will constitute approximately 15% of the course.

Reference: Class Notes

III. TOPICS:

1. Microprocessor system organisation and bus structure.
2. 8088 CPU architecture, timing and operation.
3. Analogue to Digital and Digital to Analogue converters.
4. Memory devices and memory systems used in microcomputer systems.
5. The ISA BUS and I/O subsystems
6. The logic analyser.

IV. REQUIRED RESOURCES/TEXTS/MATERIALS:

1. **Text Book:**
   - The 80x86 IBM PC and Compatible Computers (Vol I and II) by: Muhammad Ali Mazidi and Janace Gillispie Mazidi.

2. **Recommended Supplementary Reading:**
   - The 8088 and 8086 Microprocessors, Programming Interfacing, Software Hardware and Applications; by- Walter A. Triebel and Avtar Singh.

V. EVALUATION PROCESS/GRADING SYSTEM:

The mark for this course will be arrived at as follows:

3 Theory tests (20% each)	60%
Lab work, Quizzes and Assignments	40%
(The percentages shown above may have to be adjusted to accurately evaluate student skills. Students will be notified of any changes made.)	
Total	100%

80% attendance required in the labs and lectures.

- Students must complete and pass both the test and assignment portion of the course in order to pass the entire course.
- All Assignments must be completed satisfactorily to complete the course.
- Late hand in penalties will be 5% per day. Assignments will not be accepted past one week late unless there are extenuating and legitimate circumstances.
- Makeup Tests are at the discretion of the instructor and will be assigned a maximum grade of 60%.

ELIGIBILITY FOR X GRADES/UPGRADING OF INCOMPLETES

When a student's course work is incomplete or final grade is below 60%, there is the possibility of upgrading to a pass when a student meets all of the following criteria:

- The student's attendance has been satisfactory.
- An overall average of at least 50% has been achieved.
- The student has not had a failing grade in all of the theory tests taken.
- The student has made reasonable efforts to participate in class and complete assignments.

Note: **The opportunity for an X grade is usually reserved for those with extenuating circumstances.** The nature of the upgrading requirements will be determined by the instructor and may involve one or more of the following: completion of existing labs and assignments, completion of additional assignments, re-testing on individual parts of the course or a comprehensive test on the entire course.

Tests & Quizes:
Written tests will be conducted as deemed necessary; generally at the end of each block of work. They will be announced about one week in advance. Quizzes may be conducted without advance warning.

Assignments:
Assignments not completed by the due-date will be penalized by 5% per day late. All assignments must be completed satisfactorily to complete the course.

Attendance:
Attendance is mandatory. Absenteeism will affect a student's ability to succeed in this course. Absences due to medical or other unavoidable circumstances should be discussed with the instructor. There will be an attendance factor included in the lab evaluation.

The following semester grades will be assigned to students in post-secondary courses:

Grade	Definition	Grade Point Equivalent
A+	90 - 100%	4.00
A	80 - 89%	3.75
B	70 - 79%	3.00
C	60 - 69%	2.00
R (Repeat)	59% or below	0.00
CR (Credit)	Credit for diploma requirements has been awarded.	
S	Satisfactory achievement in field placement or non-graded subject areas.	
U	Unsatisfactory achievement in field placement or non-graded subject areas.	
X	A temporary grade. This is used in limited situations with extenuating circumstances giving a student additional time to complete the requirements for a course (see *Policies & Procedures Manual – Deferred Grades and Make-up*).	
NR	Grade not reported to Registrar's office. This is used to facilitate transcript preparation when, for extenuating circumstances, it has not been possible for the faculty member to report grades.	

VI. SPECIAL NOTES:

Special Needs:
If you are a student with special needs (e.g. physical limitations, visual impairments, hearing impairments, or learning disabilities), you are encouraged to discuss required accommodations with your instructor and/or the Special Needs office. Visit Room E1204 or call Extension 493, 717, or 491 so that support services can be arranged for you.

Retention of course outlines:
It is the responsibility of the student to retain all course outlines for possible future use in acquiring advanced standing at other post-secondary institutions.

Plagiarism:
Students should refer to the definition of "academic dishonesty" in *Student Rights and Responsibilities*. Students who engage in "academic dishonesty" will receive an automatic failure for that submission and/or such other penalty, up to and including expulsion from the course/program, as may be decided by the professor/dean. In order to protect students from inadvertent plagiarism, to protect the copyright of the material referenced, and to credit the author of the material, it is the policy of the department to employ a documentation format for referencing source material.

Course outline amendments:
The Professor reserves the right to change the information contained in this course outline depending on the needs of the learner and the availability of resources.

Substitute course information is available in the Registrar's office.

VII. PRIOR LEARNING ASSESSMENT:

Students who wish to apply for advanced credit in the course should consult the professor. This course is not eligible for challenge at the present time.

VIII. DIRECT CREDIT TRANSFERS:

Students who wish to apply for direct credit transfer (advanced standing) should obtain a direct credit transfer form from the Dean's secretary. Students will be required to provide a transcript and course outline related to the course in question.